

Receipt  
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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Patent Application of: Kebichi et al.

Art Unit: 2818

Application No. 09/872,212

Filed: May 31, 2001

For: SYNCHRONIZATION POINT

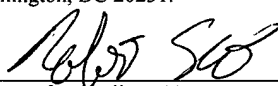
ACROSS DIFFERENT MEMORY BIST  
CONTROLLERS

Examiner: Not yet assigned

Date: October 12, 2001

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper or fee referred to as being attached or enclosed) is being deposited with the United States Postal Service on 10/12/2001 as First Class Mail in an envelope addressed to: Office of Initial Patent Examination Customer Service Center, COMMISSIONER FOR PATENTS, Washington, DC 20231.

  
Attorney for Applicant(s)REQUEST FOR CORRECTED OFFICIAL FILING RECEIPT

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Customer Service Center  
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Sir:

Applicants have received the official Filing Receipt for the application referenced above, a copy of which (with requested correction shown in red ink) is attached as Exhibit A. Attached as Exhibit B is a copy of page 1 of Applicant's patent application as filed on May 31, 2001.

The following error appears on the Filing Receipt:

**ERROR**

**Under:Domestic Priority Data -  
item omitted:**

**CORRECT INFORMATION**

**This application claims benefit of: U.S. Provisional Application No. 60/261,991 filed on January 16, 2001, which claims benefit of U.S. Provisional Patent Application No. 60/248,337, filed on November 13, 2000. This application is a continuation-in-part of U.S. Patent Application No. 09/737,620, filed on December 14, 2000.**

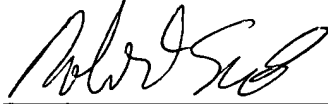
Applicants request that the identified error(s) be corrected and that a new official Filing Receipt be issued.

Please return the enclosed postcard to confirm that the items listed above have been received.

Please call the undersigned if any further information is required.

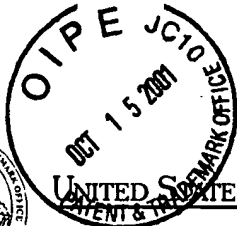
Respectfully submitted,

KLARQUIST SPARKMAN, LLP

By   
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cc: Docketing



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Commissioner for Patents  
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Mentor / RFS

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/872,212 ✓	05/31/2001 ✓	2818	1158 ✓	1011-58140 ✓	9 ✓	36 ✓	5 ✓

CONFIRMATION NO. 1993

## FILING RECEIPT



\*OC00000006371460\*

KLARQUIST SPARKMAN CAMPBELL LEIGH & WHINSTON, LLP  
One World Trade Center  
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121 S.W. Salmon Street  
Portland, OR 97204

Date Mailed: 08/01/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

## Applicant(s)

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Wu-Tung Cheng, Lake Oswego, OR; ✓  
Christopher John Hill, Hampshire, UNITED KINGDOM; ✓  
Paul J. Reuter, Northboro, MA; ✓  
Yahya M.Z. Mustafa, Wilsonville, OR; ✓

PREVIOUSLY DOCKETED

## Domestic Priority data as claimed by applicant

THIS APPLN CLAIMS BENEFIT OF 60/261,991 01/16/2001 ✓  
WHICH CLAIMS BENEFIT OF 60/248,337 11/13/2000 ✓

and U.S. Patent Application 09/737,620 12/14/2000

## Foreign Applications

If Required, Foreign Filing License Granted 08/01/2001

Projected Publication Date: Request for Non-Publication Acknowledged ✓

Non-Publication Request: Yes ✓

Early Publication Request: No ✓

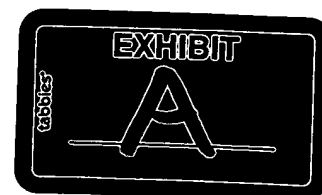
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## Title

Synchronization point across different memory BIST controllers ✓



**Preliminary Class**

365

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**Data entry by : ROBINSON, FELICIA**

**Team : OIPE**

**Date: 08/01/2001**

[REDACTED]

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Title 35, United States Code, Section 184  
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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**NOT GRANTED**

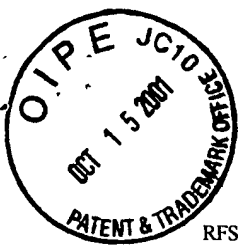
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- The articles such as "a," "an" and "the" are not included as the first words in the title of an application. They are considered to be unnecessary to the understanding of the title.
- The words "new," "improved," "improvements in" or "relating to" are not included as first words in the title of an application because a patent application, by nature, is a new idea or improvement.
- The title may be truncated if it consists of more than 500 characters (letters and spaces combined).
- The docket number allows a maximum of 25 characters.
- If your application was submitted under 37 CFR 1.10, your filing date should be the "date in" found on the Express Mail label. If there is a discrepancy, you should submit a request for a corrected Filing Receipt along with a copy of the Express Mail label showing the "date in."
- The title is recorded in sentence case.

Any corrections that may need to be done to your Filing Receipt should be directed to:

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RFS:JM:avs 1011-58140 05/31/01

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- 1 -

**SYNCHRONIZATION POINT ACROSS DIFFERENT  
MEMORY BIST CONTROLLERS**

**RELATED APPLICATION DATA**

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This application claims priority to the following U.S. applications:

- 1) U.S. Provisional Patent Application No. 60/261, 991, filed January 16, 2001.
- 2) U.S. Patent Application 09/737,620, filed December 14, 2000.
- 3) U.S. Provisional Patent Application No. 60/248,337 filed November

10 2000.

**TECHNICAL FIELD**

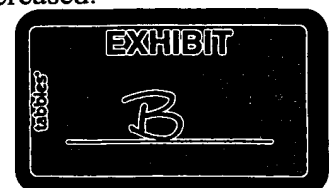
15 This invention generally relates to built-in self testing of electronic circuits and, more particularly, to built-in self testing of memory circuits such as embedded memories within an integrated circuit, memories on a multichip module, or off-chip memories.

**BACKGROUND**

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Many of today's integrated circuit (IC) designs are a complete system on a chip (SOC) that includes a processor core, multiple embedded memories, logic, I/O ports, etc. Embedded memories are the densest components in a SOC, accounting for up to 90% of the chip area. Memories are also the most sensitive to manufacturing process defects, making it essential to thoroughly test them in a SOC. As IC's are produced with greater levels of circuit density, efficient testing schemes that guarantee very high fault coverage while minimizing test costs and chip area overhead have become essential. However, as the complexity of circuits continues to increase, and as the number of memory circuits that can be packed into a chip of a given size increases, the need for efficient and cost effective testing of embedded memories has increased.

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Bib Data Sheet

CONFIRMATION NO. 1993

<b>SERIAL NUMBER</b> 09/872,212	<b>FILING DATE</b> 05/31/2001 <b>RULE</b> )	<b>CLASS</b> <del>365</del> 714	<b>GROUP ART UNIT</b> <del>2818</del> 2133	<b>ATTORNEY DOCKET NO.</b> 1011-58140
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**APPLICANTS**  
 Omar Kebichi, Wilsonville, OR;  
 Wu-Tung Cheng, Lake Oswego, OR;  
 Christopher John Hill, Hampshire, UNITED KINGDOM;  
 Paul J. Reuter, Northboro, MA;  
 Yahya M.Z. Mustafa, Wilsonville, OR;

**\*\* CONTINUING DATA \*\*\*\*\***  
 THIS APPLN CLAIMS BENEFIT OF 60/261,991 01/16/2001  
 AND A CIP OF 09/737,620 12/14/2000  
 WHICH CLAIMS BENEFIT OF 60/248,337 11/13/2000

**\*\* FOREIGN APPLICATIONS \*\*\*\*\*** YES

**IF REQUIRED, FOREIGN FILING LICENSE GRANTED**  
 \*\* 08/01/2001

Foreign Priority claimed 35 USC 119 (a-d) conditions met Verified and Acknowledged	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> Met after Allowance <i>Guy Ramane</i> Examiner's Signature Initials	<b>STATE OR COUNTRY</b> OR	<b>SHEETS DRAWING</b> 9	<b>TOTAL CLAIMS</b> 36	<b>INDEPENDENT CLAIMS</b> 5
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**TITLE**  
 Synchronization point across different memory BIST controllers

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